UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,412	09/28/2001	Richard L. Ford	042390.P11848	4354

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EXAMINER
VU, TUAN A

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 09/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/966,412	FORD, RICHARD L.
	Examiner	Art Unit
	Tuan A Vu	2124

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>28 September 2001</u>.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-28</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>1-28</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on <u>9/28/01</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   This action is responsive to the application filed September 28, 2001.

Claims 1-28 have been submitted for examination.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another
filed in the United States before the invention by the applicant for patent or (2) a patent granted on an
application for patent by another filed in the United States before the invention by the applicant for patent,
except that an international application filed under the treaty defined in section 351(a) shall have the effects
for purposes of this subsection of an application filed in the United States only if the international
application designated the United States and was published under Article 21(2) of such treaty in the English
language.

Note: 35 U.S.C. § 102(e), as revised by the AIPA and H.R. 2215, applies to all qualifying
references, except when the reference is a U.S. patent resulting directly or indirectly from
an international application filed before November 29, 2000. For such patents, the prior
art date is determined under 35 U.S.C. § 102(e) as it existed prior to the amendment by
the AIPA (pre-AIPA 35 U.S.C. § 102(e)).

3.   Claims 1-8, 10-18, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by

Pegatoquet et al., USPN: 6,598,221 (hereinafter Pegatoquet).

As per claim 1, Pegatoquet discloses a method comprising

receiving an application program, compiling the program into a first version, executing

the first compiled version by a first processor, capturing profile information during said

execution (e.g. FRONT-END: *test sequences, execution, dynamic information* – Fig. 2); and

compiling the program into a second compiled version for execution by a second

processor; the compiling of the second version including optimization based in part on the

captured profile data (e.g. *C code annotated with dynamic information, Target DSP compiler, RTL, optimized* – Fig. 2).

As per claim 2, Pegatoquet discloses captured data in memory (e.g. *basic block ... own dynamic information* – col. 7, lines 21-29; Table 1, col. 10 - Note: impart dynamic information to each basic partition of code implicitly disclose using of stored profiling results)

As per claim 3, see Pegatoquet (e.g. Fig. 2; block *30* – Fig. 1; col. 4, lines 10-25).

As per claim 4, Pegatoquet discloses dynamic information capturing tool at basic block or function level (e.g. col. 4, line 64 to col. 5, line 13; *static, dynamic* – col. 6, lines 31-54; Fig. 2; Table 1, col. 10) hence discloses monitoring instructions to direct profile capture.

As per claim 5, see DSP Fig. 2.

As per claim 6, Pegatoquet discloses front end capturing of data and DSP to received the optimized executable, i.e. DSP not able to capture profile data (Fig. 2; step 30 – Fig. 1)

As per claim 7, Pegatoquet discloses host computer to load down optimized code to a core DSP only able to function with internal buses (e.g. Fig. 1, col. 3, lines 56 to col. 4, line 9); hence discloses DSP not able to initiate external communications.

As per claim 8, Pegatoquet discloses a host processor for an simulation target system and the simulation target system includes a DSP (e.g. Fig. 1 ; *host computer*: CPU 24, *computation unit 46*)

As per claim 10, Pegatoquet discloses a one compiler to compile both profiling code and optimized code (e.g. Fig. 1, 2).

As per claim 11, this claim represents a computer-medium version of claim 1, and includes computer instructions for performing the same step limitations as recited therein; hence, is rejected using the corresponding rejections as set forth therein, respectively.

As per claims 12-18 and 20, these claims correspond to claims 2-8 and 20, respectively hence are rejected using the rejection as set forth therein, respectively.

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5.   Claims 9, 19, and 21-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pegatoquet et al., USPN: 6,598,221, as applied to claims 1(for claim 9) and 11 (for claim 19), in view of D'Arcy et al., USPN: 6,467,082 (hereinafter D'Arcy).

As per claim 9, Pegatoquet indicates the possibility to have a second compiler at the DSP level to enable manual generation of assembly code (col. 6, lines 3-17) but does not disclose having a second compiler to compile the first version of program using the profiling results. If resources permit, having more than one compiling facilities for operating a plurality of emulation/simulation target systems was a known concept which can be evidenced in D'Arcy teaching. D'Arcy, in a method to use one processor, or host, to compile code to be executed on a another processor, or target, using collection of metrics by the compiling processor analogous to Pegatoquet's host system, discloses a plurality of compilers, each for a particular operating system specific to the target system (e.g. Fig. 2B), and associating each compiler with a host

system to simulate a target processor and resolve correctness issues for the assembly targeted for

to the simulated operating system, or target platform (e.g. col. 3, lines 47-65). It would have

been obvious for one of ordinary skill in the art at the time the invention was made to provide to

the compiling resources as taught by Pegatoquet the additional compiler as taught by D'Arcy so

that for each embedded system requiring particular assembly language or operating system

specifics, a dedicated compiler as suggested by D'Arcy would enable generation of assembly

code such that all the issues related to processor or architecture specific to that target system are

easily handled without undue overhead for disassembling (see D'Arcy: col. 2, lines 27 to col. 3,

line 65).

As per claim 19, refer to claim 9 for corresponding rejection.

As per claim 21, Pegatoquet discloses a system comprising:

one or more memories, a first compiler compiling an application program into a first

compiled version (Fig. 1);

a host microprocessor executing the first compiled version, the host processor capturing

profile data during execution of the first compiled version (FRONT-END: *test sequences,*

execution, dynamic information – Fig. 2); and

a target processor (Fig. 1) and

compiling with a compiler the application code into a second compiled version, such

version being optimized based in part of the captured profile data (e.g. *C code annotated with*

dynamic information, Target DSP compiler, RTL, optimized – Fig. 2).

But Pegatoquet does not teach a second compiler for compiling the application code into

a second compiled version, the second version being optimized based on the captured profiling

data. But this limitation of having a additional compiler to compile the first version would also

have been obvious in light of the rationale as set forth in claim 9 above using D'Arcy's

teachings.

As per claims 22-25, these claims correspond to claims 2, 5, 6, and 7, respectively hence

are rejected using the rejection as set forth therein, respectively.

As per claim 26, Pegatoquet discloses a method of optimizing the execution of a

program by an embedded processor, comprising:

obtaining a program, compiling the program to generate a first set of compiled code (e.g.

Front End: *C source code, Host compiler* – Fig. 2), such code being instrumented to monitor the

execution of the first set of compiled code (e.g. col. 4, line 64 to col. 5, line 13; *static, dynamic* –

col. 6, lines 31-54; Fig. 2; Table 1, col. 10);

executing the first set of compiled code on a host processor; capturing profile

information during such execution and saving the profile information in a memory (FRONT-

END: *test sequences, execution, dynamic information* – Fig. 2);

compiling the program to generate a second set of compiled code, the second set of

compiled code being optimized based in part on the captured profile information (e.g. *C code*

annotated with dynamic information, Target DSP compiler, RTL, optimized – Fig. 2); and

executing the second set of compiled code using the embedded processor (Fig. 2; block

30 – Fig. 1; col. 4, lines 10-25).

But Pegatoquet does not disclose that the host processor is being contained in a device

that also contains the embedded processor. But according to the teachings by D'Arcy, the host

processor including capabilities of compiling, providing of target code to be executing in a target

system being in the same device as the host controller (see Fig. 2B) would enable efficient

accommodation vis-a-vis the requirements of a particular target operating system and its

execution architecture as has been mentioned in claim 9. Further, D'Arcy mentions about the

need for accommodating the increasing market requirements related to simulation of embedded

processors like DSP analogous to Pegatoquet's method (see D'Arcy: col. 1, lines 24-49) leading

to establishing a system wherein host processor includes target processor capabilities in order to

provide the support, i.e. benefits as set forth above in claim 9. Hence, for these reasons, it

would have been obvious for one of ordinary skill in the art at the time the invention was made

to provide to implement the simulation system by Pegatoquet when resources permit, such that

the host system harboring the host processor (with its compiler) also contains the embedded

target system, or DSP processing engine, for executing the compiled code provided by the host

compiler. The motivation as to why one of ordinary skill in the art would integrate both the host

system and the embedded target processor in one main simulating device would be for the same

benefits as set forth in claim 9, and additionally, by packaging a fast host processor into a same

simulation hardware embodiment as the target processor, the advantage would be that to take

advantage of the fast and powerful system of the host computer immediately available to provide

simulation or testing capabilities destined for the target system which is mostly a less capable,

embedded processor or DSP (see D'Arcy, col. 1, lines 41-48), thereby make the product more

marketable according to well-known practices such as to provide including debugging/testing

and support capabilities with the delivered software-driven product (see D'Arcy col. 1, lines 17-

32).

As per claim 27, the limitation as to use a second compiler has been addressed in claim 9 above; and is rejected herein using the corresponding rejection set forth therein.

As per claim 28, refer to claim 10 for corresponding rejection.

Conclusion

6.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (703)305-7207. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306 (for formal communications intended for entry)

or: (703) 746-8734 (for informal or draft communications, please consult Examiner before using this number)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA. , 22202. 4th Floor(Receptionist).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAT
September 4, 2004

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